What is claimed is:

1. A semiconductor device, comprising:

a gate structure located on a substrate, comprising:

a gate dielectric;

a gate electrode over the gate dielectric; and

a sidewall spacer laterally abutting the gate dielectric and the gate electrode;

a raised conductive region adjacent to and partially under the gate structure, wherein the raised conductive region comprises:

a first epitaxial-grown doped layer of the raised conductive region in contact with the substrate, the first epitaxial-grown doped layer including an elbow angle under the gate dielectric and the first epitaxial-grown doped layer interfacing the gate structure at a first point directly aligned with a vertical sidewall of the sidewall spacer contacting the gate dielectric;

a second epitaxial-grown doped layer on the first epitaxial-grown doped layer and including a same dopant species as the first epitaxial-grown doped layer, wherein the second epitaxial-grown doped layer having a higher dopant concentration than the first epitaxial-grown doped layer, the second epitaxial-grown doped layer interfacing the gate structure along a bottom of the sidewall spacer from the first point to a second point under the bottom of the sidewall spacer away from the first point and the gate dielectric; and

a third epitaxial-grown doped layer on the second epitaxial-grown doped layer and including the same dopant species as the first epitaxial-grown doped layer, wherein the third epitaxial-grown doped layer comprises a higher dopant concentration than the second epitaxial-grown doped layer, and the third epitaxial-grown doped layer interfacing the gate structure at least at the second point,

wherein the dopant concentration is constant throughout each of the epitaxial-grown doped layers.

2. The semiconductor device of claim 1, wherein the first epitaxial-grown doped layer comprises a first vertical thickness and the second epitaxial-grown doped layer comprises a second vertical thickness, and a ratio between the second vertical thickness and the first vertical thickness is greater than about 0.8.

3. The semiconductor device of claim 2, wherein the third epitaxial-grown doped layer comprises a third vertical thickness, and a ratio between the third vertical thickness and a combination of the first vertical thickness and the second vertical thickness is less than about 0.5.

4. The semiconductor device of claim 1, wherein a central portion of the third epitaxial-grown doped layer raises from a surface of the substrate.

5. The semiconductor device of claim 1, wherein the first epitaxial-grown doped layer is a U-shaped structure in the substrate.

6. The semiconductor device of claim 1, wherein the first epitaxial-grown doped layer comprises an epitaxial semiconductor material that is the same as that of the second epitaxial-grown doped layer and the third epitaxial-grown doped layer.

7. The semiconductor device of claim 1, wherein the first epitaxial-grown doped layer comprises a dopant concentration ranging from about 1e19 atoms per cm^3 to about 2e20 atoms per cm^3, the second epitaxial-grown doped layer comprises a dopant concentration ranging from about 2e20 atoms per cm^3 to 6e20 atoms per cm^3, and the third epitaxial-grown doped layer comprises a dopant concentration ranging from about 6e20 atoms per cm^3 to 2e21 atoms per cm^3.

8. The semiconductor device of claim 1, wherein the first epitaxial-grown doped layer is separated from the third epitaxial-grown doped layer by the first point and the second point.

9. The semiconductor device of claim 1, wherein the first point is separated from the second point by a width of from about 1 angstrom to about 100 angstrom.

10. The semiconductor device of claim 1, wherein the elbow angle of the first epitaxial-grown doped layer is not interfacing with the gate structure.

11. The semiconductor device of claim 1, wherein a separation between the first point and the second point is less than a width of the sidewall spacer.

12. A semiconductor structure, comprising:

a gate structure located on a substrate, comprising:

a gate dielectric;

a gate electrode over the gate dielectric; and

a sidewall spacer laterally abutting the gate dielectric and the gate electrode;

a raised conductive region adjacent to and partially under the gate structure, wherein the raised conductive region comprises:

a first epitaxial-grown doped liner of the raised conductive region in contact with the substrate, comprising a first lateral thickness and a first vertical thickness, a ratio between the first lateral thickness and the first vertical thickness being less than about 1, the first epitaxial-grown doped liner including an elbow angle under the gate dielectric and the first epitaxial-grown doped liner interfacing the gate structure at a first point aligned with a vertical sidewall of the sidewall spacer contacting the gate dielectric;

a second epitaxial-grown doped liner on the first epitaxial-grown doped liner, the second epitaxial-grown doped liner interfacing the gate structure along a bottom of the sidewall spacer from the first point to a second point under the bottom of the sidewall spacer away from the first point and the gate dielectric, a separation between the first point and the second point comprising a second lateral thickness; and

a third epitaxial-grown doped liner on the second epitaxial-grown doped liner, the third epitaxial-grown doped liner interfacing the gate structure at least at the second point,

wherein the dopant concentration is constant throughout each of the epitaxial-grown doped layers.

13. The semiconductor device of claim 12, wherein a ratio between the second lateral thickness and a second vertical thickness of the second epitaxial-grown doped liner is in a range from about 0.5 to about 1.

14. The semiconductor device of claim 12, wherein the second lateral thickness of the second epitaxial-grown doped liner is in a range from about 50 angstroms to 200 angstroms.

15. The semiconductor device of claim 12, wherein the third epitaxial-grown doped liner comprises a dopant concentration from about 10 to 100 times higher than that of the second epitaxial-grown doped liner.

16. The semiconductor device of claim 12, wherein the second epitaxial-grown doped liner is configured to prevent dopant diffusion between the third epitaxial-grown doped liner and the substrate.

17. The semiconductor device of claim 12, wherein the second epitaxial-grown doped liner is configured to prevent lateral dopant diffusion between the third epitaxial-grown doped liner and the channel region.